3 T835 Initial Tuning & Adjustment

The following section describes the full tuning and adjustment procedure and provides information on:

- channel programming
- channel selection
- selecting required audio links
- synthesiser alignment
- receiver front end and IF alignment
- noise mute adjustment
- setting line output level
- setting monitor output level
- setting up the RSSI
- carrier level mute adjustment.

3.1 Channel Programming

Up to 128 channel frequencies can be stored in the EPROM memory (IC1). Each channel can be addressed using the bank of 8 switches (SW1). The most significant bit of this switch is set according to the type of EPROM fitted:

ON = 27C16
OFF = 27C64

Up to 8 channels may be addressed externally when the optional extra rear D-range connector is fitted.

Programming is accomplished by using an IBM[1] PC, a PROM programmer and the PGM800 software package. For a full description of the programming procedure, refer to the T800 Programming Software User's Manual.

3.2 DIP Switch Codes For Channel Addresses

The PGM800 software used to programme the EPROM will present the user with a DIP switch code for each channel address (refer to Section 3.11). For example, channel 125 will be assigned a switch code of X0000011 (1-128 channel numbering), in which case the switches should be set as shown in Figure 3.1, i.e. **0**0000011.

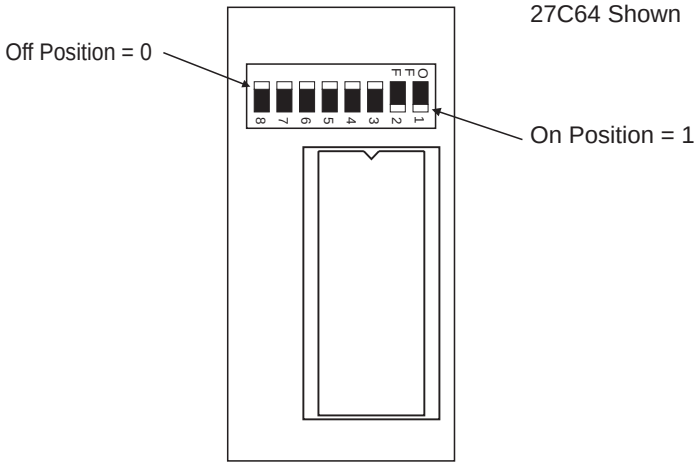

Figure 3.1 Channel DIP Switch Setting

Note 1: For remote multichannel applications using the T800-07 multichannel memory PCB, the DIP switch is not used and should have the first 3 least significant bits (1-3) in the ***off*** position. The next 4 bits (4-7) should be ***on***, while the most significant bit (8) is selected according to the EPROM used (refer to Section 3.1). This will allow the existing CHSEL lines to be used to select up to 8 channels. It is possible to address blocks of 8 channels throughout the 128 channel EPROM capacity by switching bits 4 to 7 on the DIP switch.

Note 2: Alternatively, all 128 channels may be remotely addressed on the T800-07, but bits 1-7 of the DIP switch should be in the ***off*** position. In this case it will be necessary to drill a hole to route the 7 channel select lines from the synthesiser compartment to the D-range connector. Later models have an access slot between these two compartments.

1. IBM is a registered trademark of International Business Machines.

3.3 Audio Processor Links

3.3.1 General

The links available for various circuit block options are listed by function as follows:

Plug	Link	Function
PL100	1 - 2 2 - 3	Rx disable link not connected
PL101	1 - 2 2 - 3	flat response de-emphasised response
PL102	1 - 2 2 - 3	relay link not connected
PL103	1 - 2 2 - 3	de-emphasised response flat response
PL104	1 - 2 2 - 3	noise mute carrier mute
PL105*	1 - 2 2 - 3 or 3 - 4 4 - 5	bypass high pass filter 300Hz high pass filter in circuit audio input via audio 2 or 3
PL106	1 - 2 2 - 3	audio input via audio 2 pad audio input via audio 3 pad

*Refer to Section 3.3.2 for further details.

The required options should be selected before alignment of the receiver is attempted.

3.3.2 Audio Processor Linking Details For CTCSS

The audio processor links must be appropriately connected for the CTCSS option used, as shown in the table below.

CTCSS Option	PL105	PL106
standard, no CTCSS	2 - 3	2 - 3
CTCSS tone + speech to line output	1 - 2	2 - 3
internal CTCSS	4 - 5	2 - 3
external CTCSS	4 - 5	1 - 2

The conditions stated in the above table are defined as follows:

- standard, no CTCSS
  - CTCSS or other sub-audio signalling used
  - audio bandwidth 300Hz to 3kHz
  - hum & noise -55dB
- CTCSS tone + speech to line output
  - tone and speech transmitted down 600 ohm line
  - audio bandwidth 10Hz to 3kHz
  - hum & noise -45dB
  - decoding performed in exciter / transmitter
- internal CTCSS
  - decoding performed in receiver by T800-02 or similar
  - re-encoded tone output via "audio 2", speech sent down 600 ohm line
- external CTCSS
  - decoding performed through the receiver (but externally) by T310-05 or similar
  - speech injected back into receiver via "audio 2" and sent down 600 ohm line

3.4 Test Equipment Set-up

Set up the test equipment as shown below:

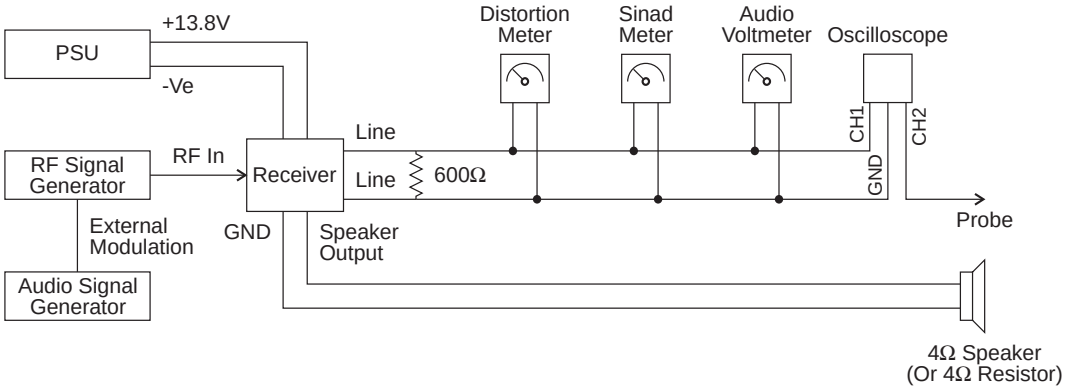

Figure 3.2 Test Equipment Set-up

3.5 Synthesiser Alignment

- Ensure that the EPROM (IC1) has been programmed with the required frequencies using PGM800 software.

- **Single Channel** Select a channel on the EPROM PCB DIP switch.

  Multichannel Select the middle channel via the EPROM PCB DIP switch.

  If there is no channel near the middle of the required switching range, it may be necessary to programme an additional channel specifically for alignment purposes.

- Connect a high impedance voltmeter to PL4-1 or the junction of L1 & R1 in the VCO (this measures the synthesiser loop voltage).

- **Single Channel** Tune VCO trimmer VC1 for a synthesiser loop voltage of 9V.

  Multichannel Tune VCO trimmer VC1 for a synthesiser loop voltage of 9V on the middle channel.

  All channels should lie within the upper and lower limits of 13V and 5V respectively.

  Do not attempt to programme channels with a greater frequency separation than the specified switching range of 3MHz.

- The TCXO (IC2) output frequency should be trimmed when the IF is tuned - refer to Section 3.6.

3.6 Alignment Of Receiver Front End And IF

Note 1: In this and following sections deviation settings are given first for wide band sets, followed by settings in brackets for narrow band sets [ ].

Note 2: **Frequency Range**

136-156MHz: With the power supply switched off, solder bridge links 1-6 and link B in the front end.

148-174MHz: Solder bridge link A and ensure links 1-6 and link B are not connected.

Align the synthesiser as instructed in Section 3.5. For multichannel operation the receiver should be aligned on a frequency in the middle of the required band.

Inject a strong on-channel RF signal with 3kHz deviation [1.5kHz] at 1kHz into the antenna socket and adjust L304, L305, L309 & L310 to give best sinad.

Continually decrease the RF level to maintain 12dB sinad.

Roughly tune IF coils L315/L316/L317, VC301 and quad coil L319 for best sinad.

While maintaining a low level unmodulated RF input to the receiver, loosely couple into the first IF an additional high level signal at 21.4MHz - a beat note will be heard.

Trim the synthesiser TCXO (IC2) for zero beat.

Readjust the front end doublets (L304, L305, L309 & L310) to give best sinad.

Change the RF signal level to -75dBm and modulate with 3kHz deviation [1.5kHz] at 1kHz.

Connect an oscilloscope probe to the RSSI test point (pad 115 or 125) and connect plugs PL101 and PL103 to give a flat audio response (refer to Section 3.3).

Readjust IF coils L315/L316/L317, VC301 and quad coil L319 to give a maximum amplitude response on the oscilloscope with minimal amplitude modulation.

Further adjust these coils, along with L319, for minimum audio distortion, ensuring that the 455kHz level (on the oscilloscope) does not fall significantly.

Check that the distortion reading is less than 2%.

Reconnect plugs PL101 and PL103 to give a de-emphasised audio response (if required) and reduce the RF level until 12dB sinad is reached. The receiver sensitivity should be better than -117dBm, assuming that the audio levels are not being overdriven (refer to Section 3.8).

3.7 Noise Mute Adjustment

Connect pins 1 & 2 of PL104 to enable the noise mute.

Align the receiver as instructed in Section 3.5 and Section 3.6.

Set the RF level to -105dBm with 3kHz deviation [1.5kHz] at 1kHz.

Set RV100 (gate sensitivity) fully anticlockwise.

Adjust RV301 to close the mute (if necessary turn off the RF signal and then turn it on again).

Rotate RV301 anticlockwise until the mute just opens.

Once the mute has been set up as described above, RV100 (gate sensitivity) on the front panel may be adjusted for the required opening sinad.

3.8 Audio Processor

3.8.1 Line Amplifier Output

Apply an on-channel signal from the RF generator at a level of -70dBm with 3kHz deviation [1.5kHz] at 1kHz.

Adjust the front panel line level pot. (RV102) to give an output of +10dBm on the 600 ohm line.

Check for any clipping or distortion on the oscilloscope.

Set the line level to the required output level.

3.8.2 Monitor Amplifier Output (Speaker Output)

Adjust the front panel monitor volume control (RV103) to give an output of 2V rms into a 3.5 ohm resistive load.

Check for any clipping or distortion on the oscilloscope.

Switch to a 3.5 ohm speaker load and adjust RV103 to the required level.

3.9 RSSI

Align the receiver as instructed in Section 3.5 and Section 3.6.

Apply an on-channel signal from the RF generator at a level of -100dBm with 3kHz deviation [1.5kHz] at 1kHz.

Adjust RV303 to give 4.5V RSSI output on pin 5 on the rear D-range connector when measured with a high impedance DMM.

3.10 Carrier Level Mute

Connect pins 2 and 3 of PL104 to enable the carrier mute and disable the noise mute.

Apply an on-channel signal from the RF generator at the required mute opening level with 3kHz deviation [1.5kHz] at 1kHz.

Adjust the carrier mute pot. (RV104) to close the mute (if necessary, momentarily turn off the RF), then slowly adjust it until the mute just opens. The mute should now open at this preset level.

3.11 PGM800 DIP Switch Codes

PGM800 channel numbers can range from 0-127 or 1-128, depending on which version you are using:

Version	Channel Numbers
V2 and earlier	0-127
V2.01	1-128
V2.21 and later	0-127 or 1-128

The following sections provide DIP switch code lists for both numbering systems.

3.11.1 DIP Switch Codes For Channel Numbers 0-127

0 = off 1 = on

Channel	DIP Code	Channel	DIP Code	Channel	DIP Code
0	X1111111	45	X1010010	90	X0100101
1	X1111110	46	X1010001	91	X0100100
2	X1111101	47	X1010000	92	X0100011
3	X1111100	48	X1001111	93	X0100010
4	X1111011	49	X1001110	94	X0100001
5	X1111010	50	X1001101	95	X0100000
6	X1111001	51	X1001100	96	X0011111
7	X1111000	52	X1001011	97	X0011110
8	X1110111	53	X1001010	98	X0011101
9	X1110110	54	X1001001	99	X0011100
10	X1110101	55	X1001000	100	X0011011
11	X1110100	56	X1000111	101	X0011010
12	X1110011	57	X1000110	102	X0011001
13	X1110010	58	X1000101	103	X0011000
14	X1110001	59	X1000100	104	X0010111
15	X1110000	60	X1000011	105	X0010110
16	X1101111	61	X1000010	106	X0010101
17	X1101110	62	X1000001	107	X0010100
18	X1101101	63	X1000000	108	X0010011
19	X1101100	64	X0111111	109	X0010010
20	X1101011	65	X0111110	110	X0010001
21	X1101010	66	X0111101	111	X0010000
22	X1101001	67	X0111100	112	X0001111
23	X1101000	68	X0111011	113	X0001110
24	X1100111	69	X0111010	114	X0001101
25	X1100110	70	X0111001	115	X0001100
26	X1100101	71	X0111000	116	X0001011
27	X1100100	72	X0110111	117	X0001010
28	X1100011	73	X0110110	118	X0001001
29	X1100010	74	X0110101	119	X0001000
30	X1100001	75	X0110100	120	X0000111
31	X1100000	76	X0110011	121	X0000110
32	X1011111	77	X0110010	122	X0000101
33	X1011110	78	X0110001	123	X0000100
34	X1011101	79	X0110000	124	X0000011
35	X1011100	80	X0101111	125	X0000010
36	X1011011	81	X0101110	126	X0000001
37	X1011010	82	X0101101	127	X0000000
38	X1011001	83	X0101100		
39	X1011000	84	X0101011		
40	X1010111	85	X0101010		
41	X1010110	86	X0101001		
42	X1010101	87	X0101000		
43	X1010100	88	X0100111		
44	X1010011	89	X0100110		

3.11.2 DIP Switch Codes For Channel Numbers 1-128

0 = off 1 = on

Channel	DIP Code	Channel	DIP Code	Channel	DIP Code
1	X1111111	46	X1010010	91	X0100101
2	X1111110	47	X1010001	92	X0100100
3	X1111101	48	X1010000	93	X0100011
4	X1111100	49	X1001111	94	X0100010
5	X1111011	50	X1001110	95	X0100001
6	X1111010	51	X1001101	96	X0100000
7	X1111001	52	X1001100	97	X0011111
8	X1111000	53	X1001011	98	X0011110
9	X1110111	54	X1001010	99	X0011101
10	X1110110	55	X1001001	100	X0011100
11	X1110101	56	X1001000	101	X0011011
12	X1110100	57	X1000111	102	X0011010
13	X1110011	58	X1000110	103	X0011001
14	X1110010	59	X1000101	104	X0011000
15	X1110001	60	X1000100	105	X0010111
16	X1110000	61	X1000011	106	X0010110
17	X1101111	62	X1000010	107	X0010101
18	X1101110	63	X1000001	108	X0010100
19	X1101101	64	X1000000	109	X0010011
20	X1101100	65	X0111111	110	X0010010
21	X1101011	66	X0111110	111	X0010001
22	X1101010	67	X0111101	112	X0010000
23	X1101001	68	X0111100	113	X0001111
24	X1101000	69	X0111011	114	X0001110
25	X1100111	70	X0111010	115	X0001101
26	X1100110	71	X0111001	116	X0001100
27	X1100101	72	X0111000	117	X0001011
28	X1100100	73	X0110111	118	X0001010
29	X1100011	74	X0110110	119	X0001001
30	X1100010	75	X0110101	120	X0001000
31	X1100001	76	X0110100	121	X0000111
32	X1100000	77	X0110011	122	X0000110
33	X1011111	78	X0110010	123	X0000101
34	X1011110	79	X0110001	124	X0000100
35	X1011101	80	X0110000	125	X0000011
36	X1011100	81	X0101111	126	X0000010
37	X1011011	82	X0101110	127	X0000001
38	X1011010	83	X0101101	128	X0000000
39	X1011001	84	X0101100		
40	X1011000	85	X0101011		
41	X1010111	86	X0101010		
42	X1010110	87	X0101001		
43	X1010101	88	X0101000		
44	X1010100	89	X0100111		
45	X1010011	90	X0100110		